**CPE 343 – Computer Organization & Architecture**

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**Lab # 1**

**Title: Introduction to VHDL and Quatus2 with the design and combinational circuits.**

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**INTRODUCTION:**

**VHDL:** It is the hardware descriptive language used in electronic design automation to describe digital and mixed-signal systems. VHDL is also used as a general purpose parallel programing language.

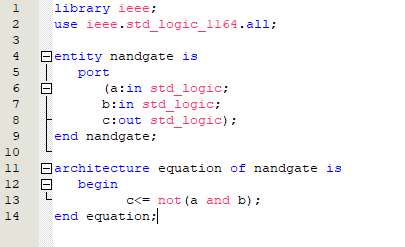
**Quatus:** It is the platform design environment that easily adapts to your specific needs in all FPGA’s design.

It takes VHDL code and complies it into gate level diagram and then optimize for its performance.

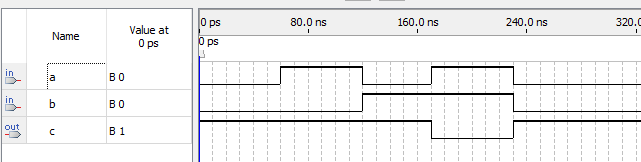
**LAB TASKS: (In-Lab Tasks)**

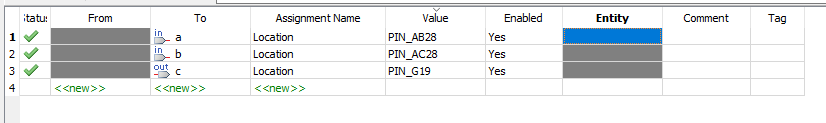
**Task 1:**

1. VHDL Code



1. Results (VWF)





# CONCLUSION:

In this lab I learned about

* The basics of VHDL code

1. Library
2. Entity
3. Architecture

* Quatus

1. Creating project
2. Simulating VHDL code.